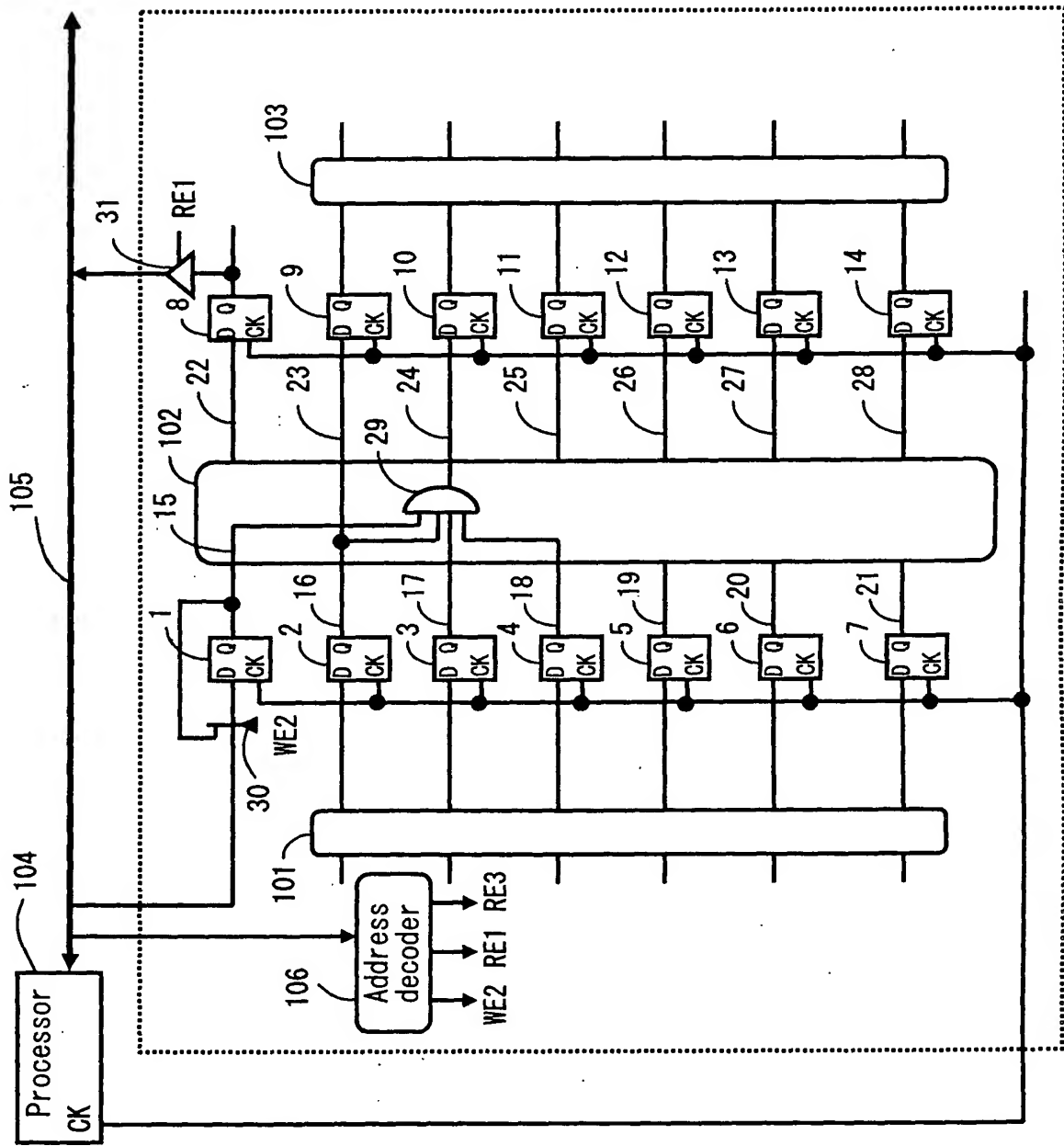


CO



15 

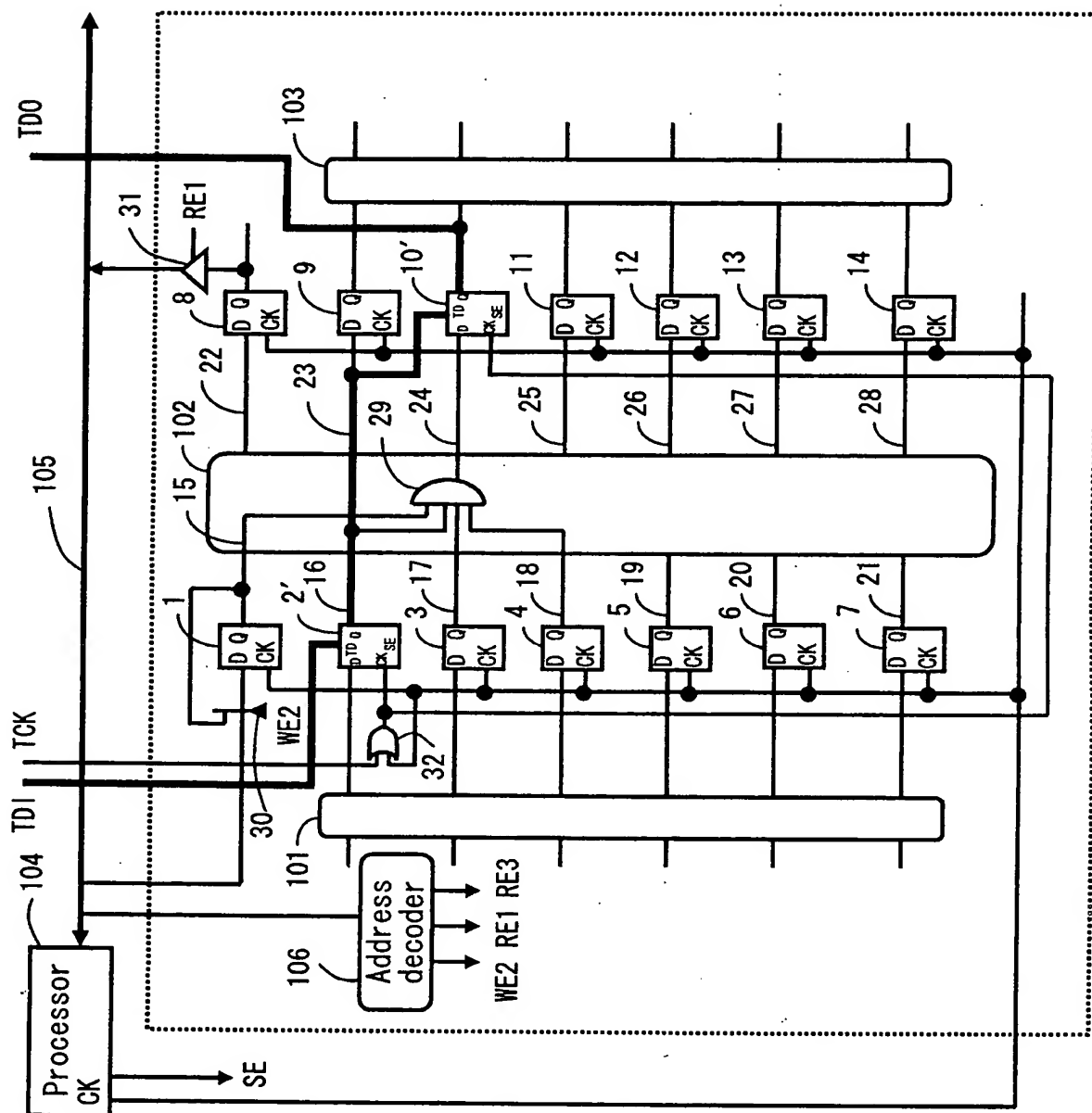


FIG. 3A

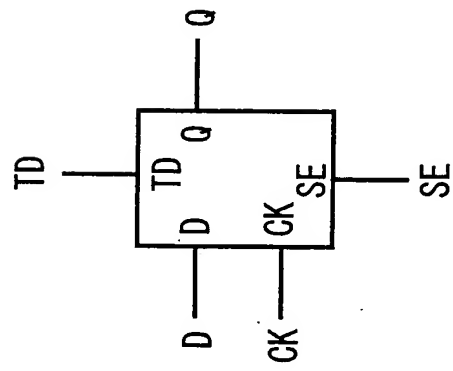


FIG. 3B

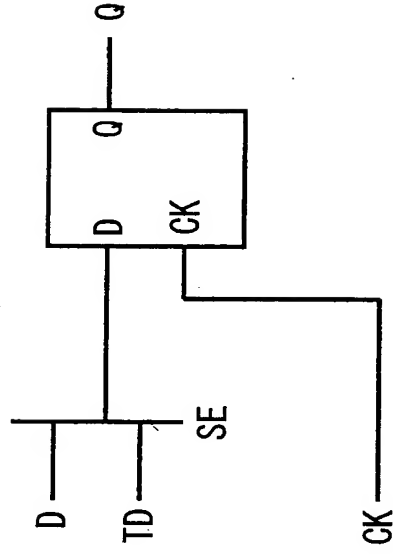


FIG. 4

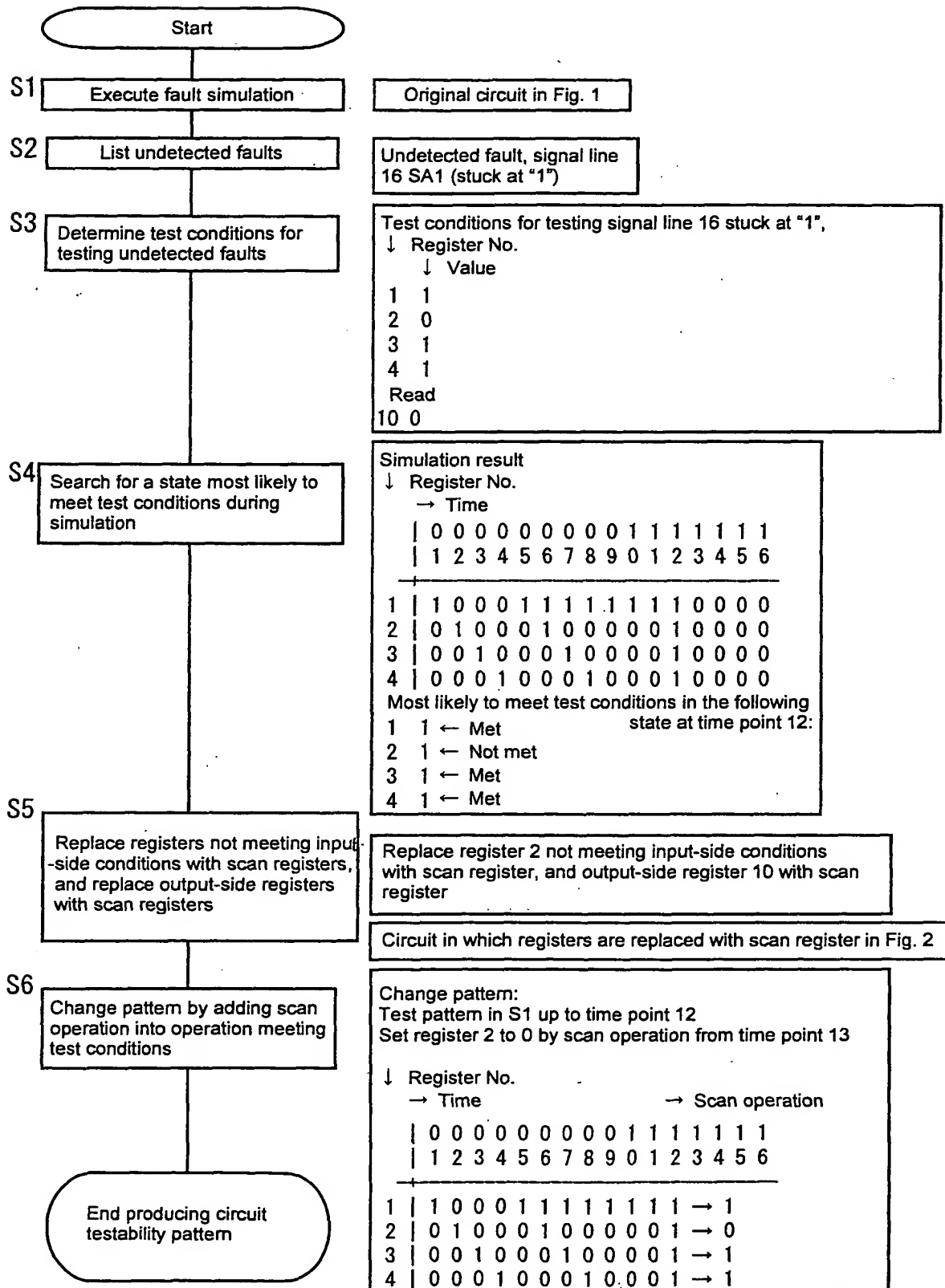


FIG. 5

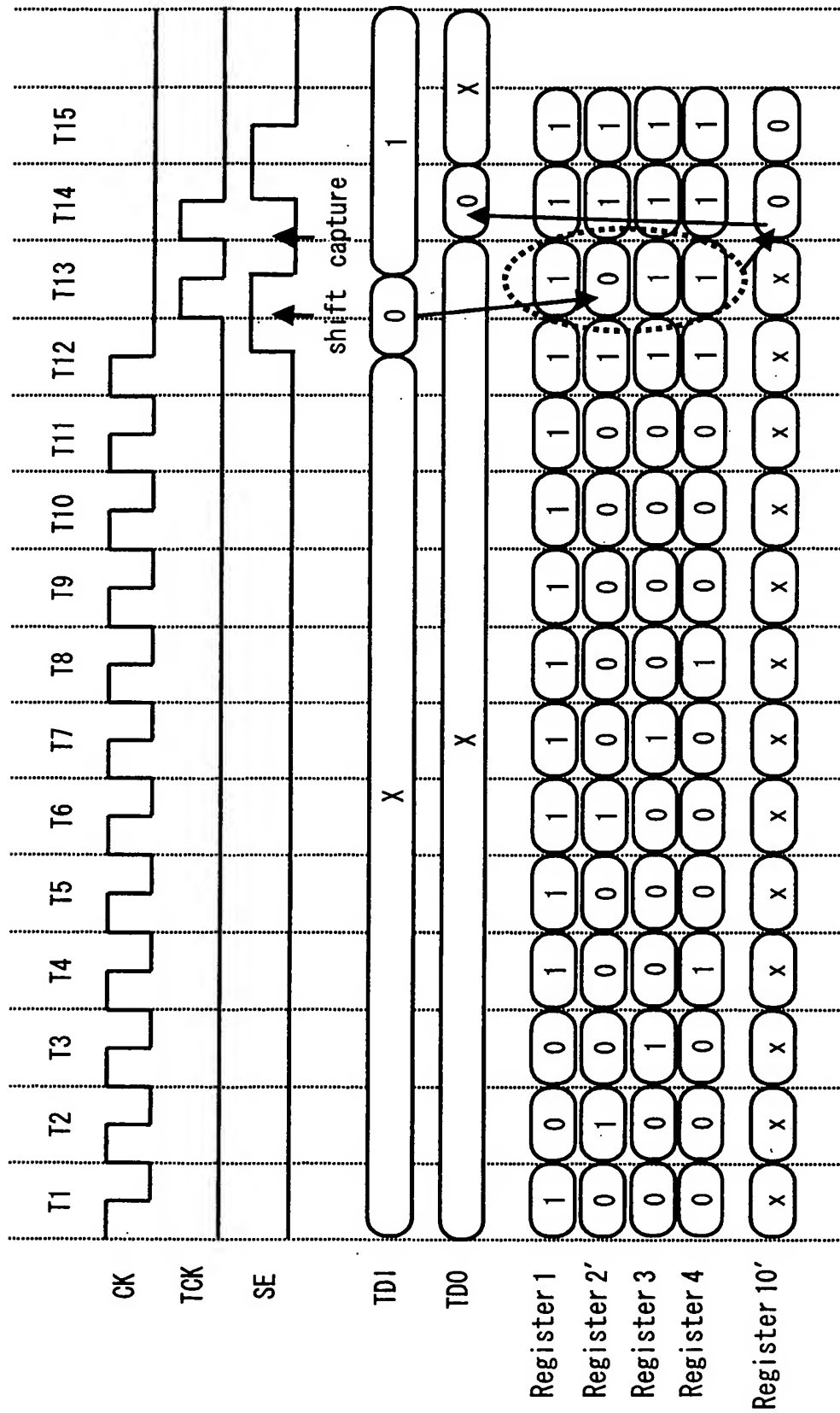


FIG. 6

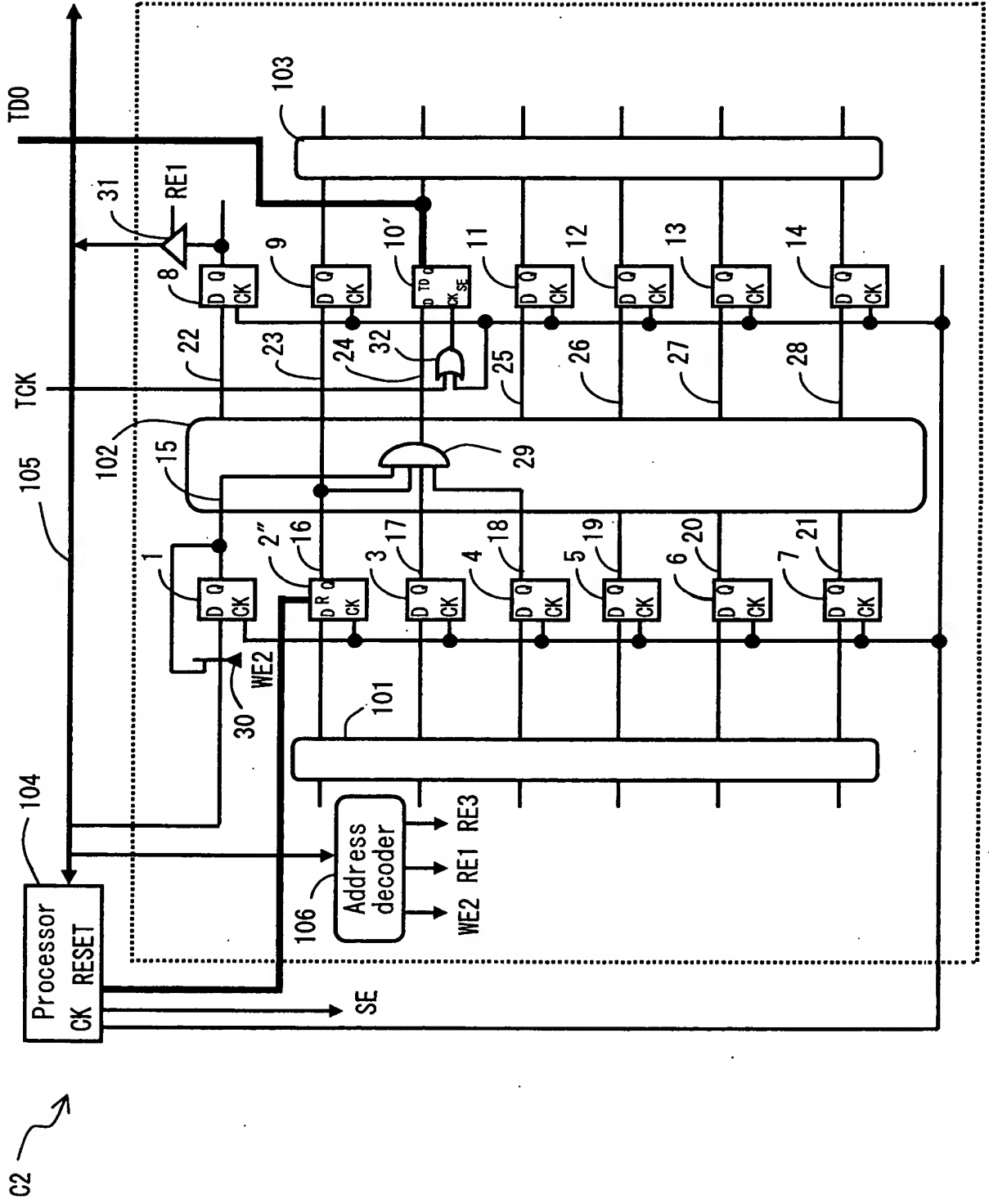
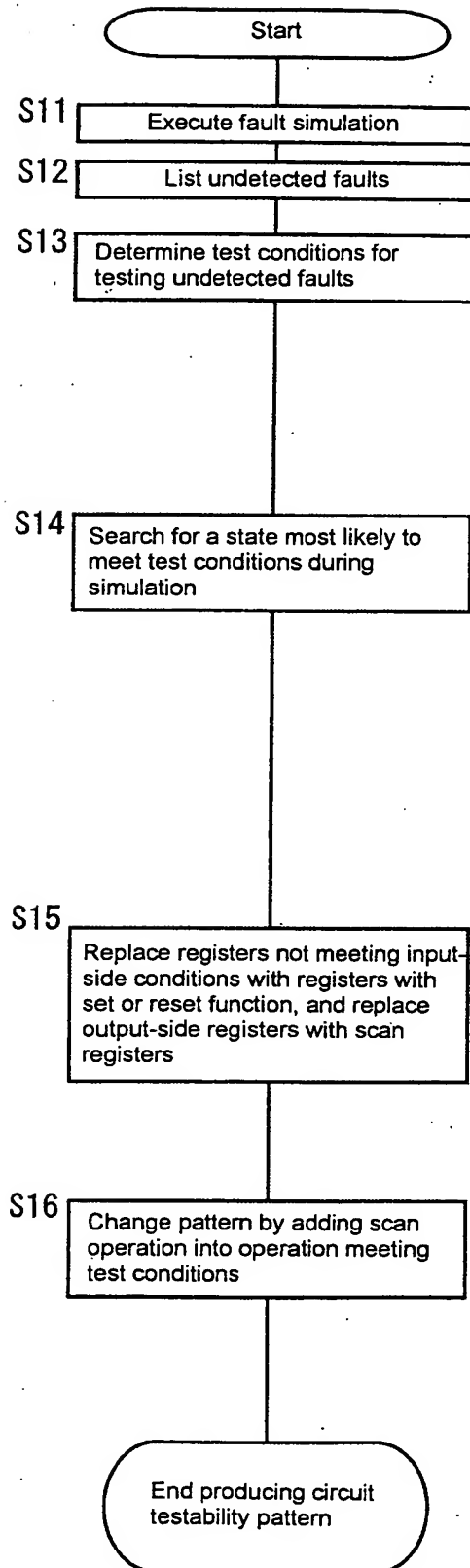


FIG. 7



Original circuit in Fig. 1

Undetected fault, signal line 16 SA1 (stuck at "1")

Test conditions for testing signal line 16 stuck at "1",

↓ Register No.

↓ Value

1 1

2 0

3 1

4 1

Read

10 0

Simulation result

↓ Register No.

→ Time

	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6

1	1	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
2	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0
3	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
4	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0

Most likely to meet test conditions in the following state at time point 12:

1 1 ← Met
 2 1 ← Not met
 3 1 ← Met
 4 1 ← Met

Replace register 2 not meeting input-side conditions with register with reset function, and output-side register 10 with scan register. Though only one in this case, registers with reset function, registers with set function and registers in scan chain may be plural in number

Circuit in which registers are replaced by register with set/reset function and scan register in Fig. 6

Change pattern:

Test pattern in S11 up to time point 12

Set register 2 to 0 by reset operation at time point 13.

Observe result by scan operation.

↓ Register No.

Reset operation

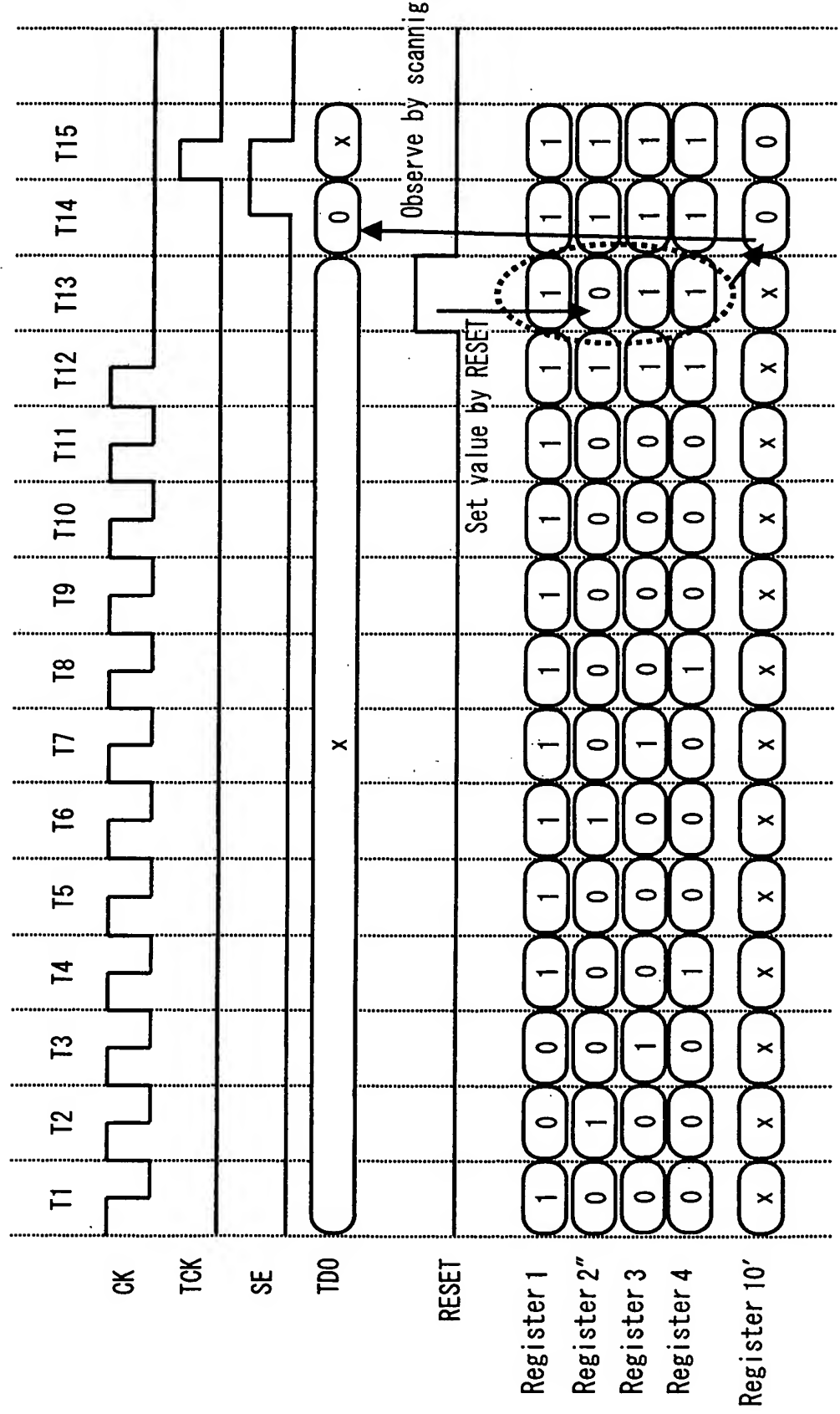
→ Time

→ Scan operation

	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6

1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	→ 1
2	0	1	0	0	0	1	0	0	0	0	0	1	→ 0			
3	0	0	1	0	0	0	1	0	0	0	0	1	→ 1			
4	0	0	0	1	0	0	0	1	0	0	0	1	→ 1			

FIG. 8



3

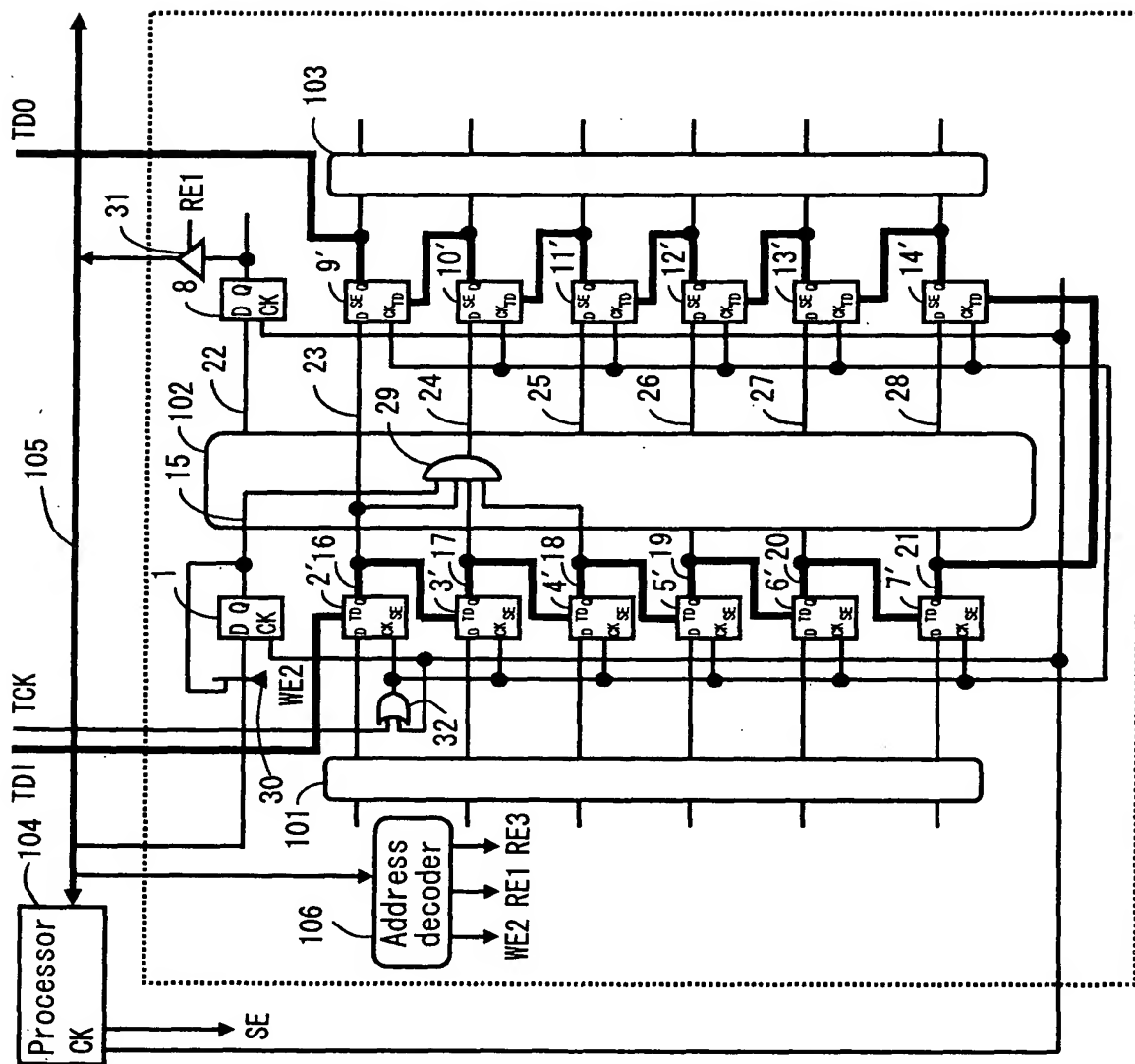


FIG. 10

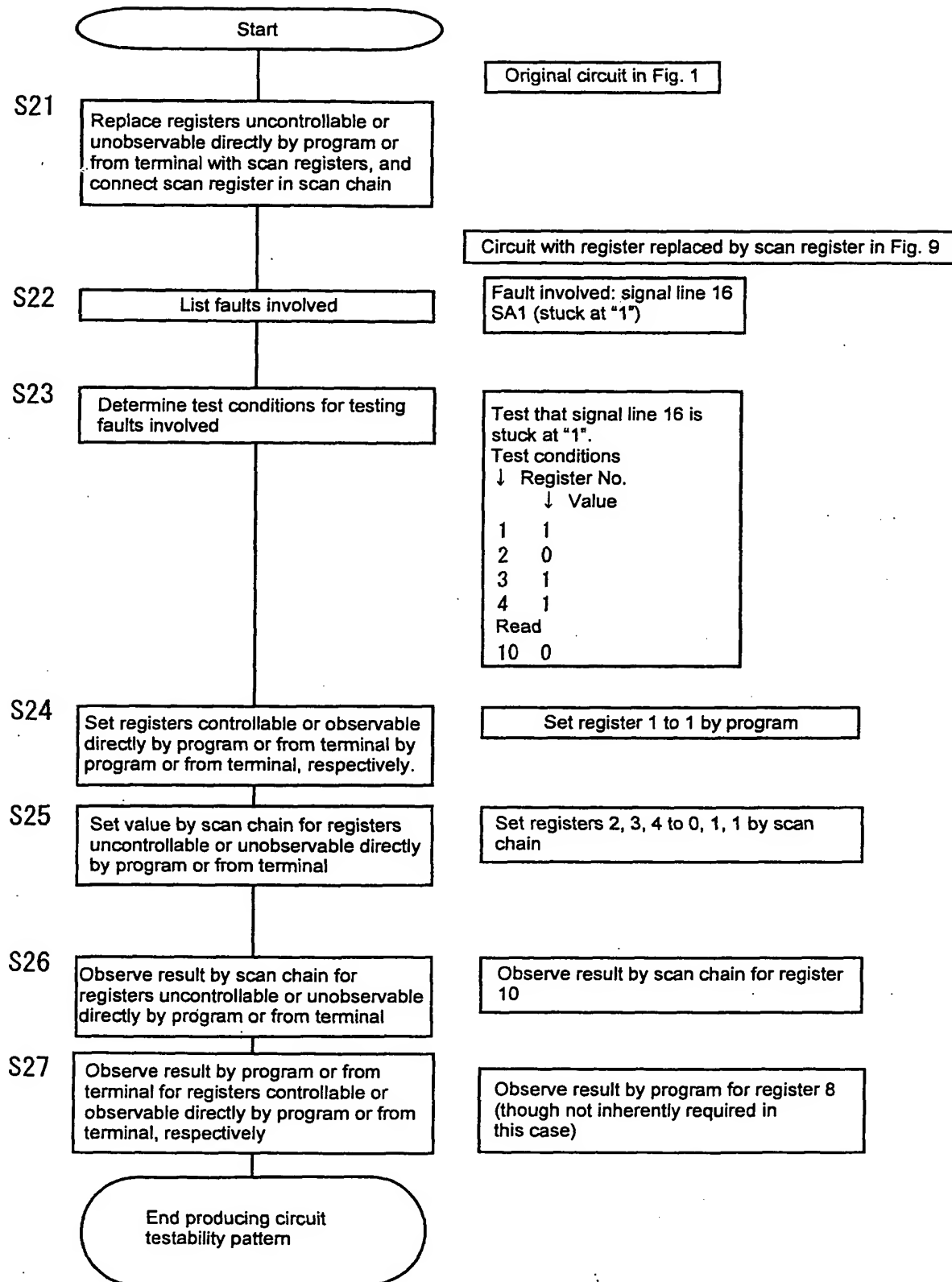


FIG. 11

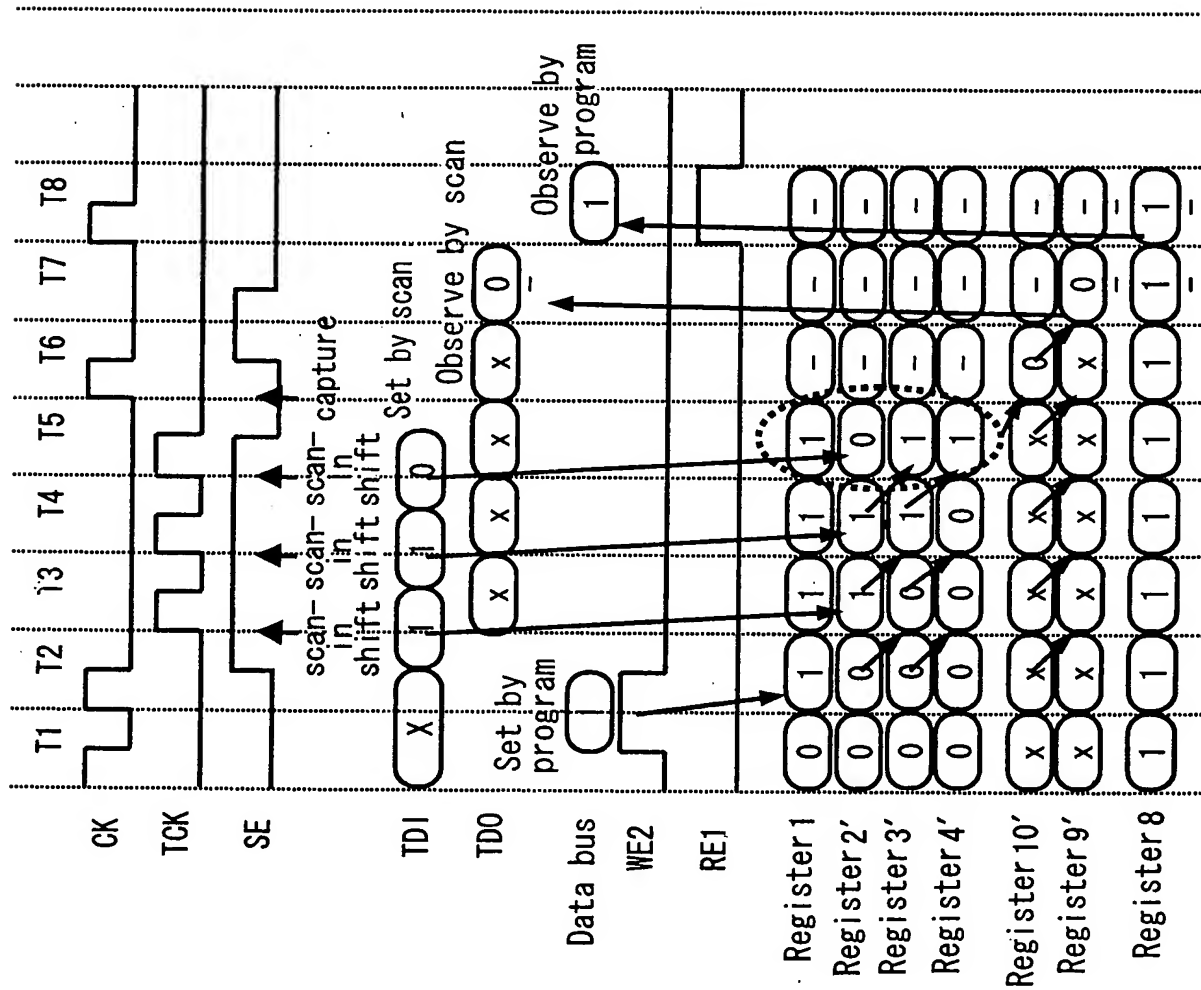


FIG. 12

